

## PROTECTION OF INTEGRATED CIRCUIT GATES DURING METALLIZATION PROCESSES

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### CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/458,047, entitled "Novel Gate Protection Technique Against Charge Buildup," filed on March 27, 2003 by Sanjay Rekhi, Nagendra Cherukupalli, and Paul Keswick, incorporated herein  
10 by reference in its entirety.

### BACKGROUND OF THE INVENTION

#### 1. Field Of The Invention

The present invention relates generally to semiconductor devices, and more  
15 particularly but not exclusively to the protection of integrated circuit gates during fabrication.

#### 2. Description of the Background Art

In the manufacture of semiconductor devices, physical vapor deposition (PVD, also known as sputtering) is commonly used to deposit thin films of metal on a silicon  
20 substrate. This process involves conversion of target material into vapor phase by ion bombardment. The bombarding ion used is typically an inert gas, such as Argon. The property of inertness is important because it does not react with other species. In order for material to become a bombarding species it must gain sufficient energy and be

directed towards a target metal. The inert gas atoms gain sufficient energy through the ionization process in a plasma. A plasma or glow discharge is an energetic ionized gas generated by electric discharge in a gaseous medium. The PVD process may take ten to thirty seconds, so voltage buildup may be in the order of tens of volts in the last few  
5 seconds of the process. A PVD process in one exemplary embodiment is schematically illustrated in FIG. 1, where plasma 112 allows for deposition of metal from a target 110 onto a silicon wafer substrate 114. During this processing step, relatively high charges can buildup on existing metal layers on the silicon substrate.

As process technology advances and gate oxides of transistors are scaled down,  
10 breakdown of the oxide and reliability become a concern. Higher electric fields in the oxide increase the tunneling of carriers from the channel into the oxide, causing a charge buildup. Since the gate oxide is relatively thin, this charge buildup can destroy the gate oxide, thereby degrading transistor performance. FIG. 2 schematically illustrates this charge buildup on a gate of a logic module 103. Logic modules 102 and  
15 103 may be part of a multi-level device. In the example of FIG. 2, interconnect lines 104 and 106 may be formed on a first metal level (also referred to as "M1"), while interconnect line 105 may be formed on a second metal level (also referred to as "M2") above the first metal level. The formation of interconnect line 105 by PVD may result in charge buildup on interconnect line 106, which may damage module 103 and other  
20 circuits connected to interconnect line 106. This is a problem in semiconductor manufacturing processes, and may result in low yield.

A conventional technique to guard against damage to gates due to charge buildup is shown in the schematic diagram of FIG. 3. The conventional technique

involves the use of reverse bias diodes, where the reverse breakdown and leakage characteristics are relied upon to discharge the accumulated charge on the gates. In FIG. 3, a diode 302 serves to protect the gate of transistor 303 from charge buildup on interconnect line 301 during a PVD process. To be effective, this technique may require

5 the use of many diodes per interconnect line (also referred to as a "net" in a layout).

The graph of FIG. 4 shows the number of diodes (also referred to as "antenna cells" or "antenna diodes") as a function of a number of nets for an example device. The first data point indicates there are 97 nets that require only 1 diode, the last data point indicates there are 6 nets that require 25 diodes, and data point 410 indicates that there

10 are 3 nets that require 23 diodes. FIG. 5 schematically shows a layout of a conventional solution showing the relatively high number of diode cells 504 required in one exemplary embodiment. In the example of FIG. 5, five diode cells 504 protect a gate (not shown) connected to interconnect line 502, which in turn is coupled to diode cells 504 by way of interconnect lines 506 and 508. FIG. 6 shows the equivalent

15 schematic diagram for diode cells 504. The ratio of the amount of metal area of the interconnect line to the amount of gate area to be protected determines how many diodes need to be placed on the interconnect line. Many diodes may need to be placed on long nets. These diodes load the net and continue to leak charge even during normal operation. They are costly in terms of area, power and signal propagation delay.

## 20 SUMMARY

In one embodiment, a first transistor is configured to switch ON to discharge accumulated charges on an interconnect line during a metallization process. This

advantageously protects a second transistor, which is coupled to the interconnect line, from charge buildup. The gate of the first transistor may be coupled to the interconnect line by way of a coupling capacitor. The gate of the first transistor may remain floating during the metallization process, and subsequently coupled to ground at a topmost  
5 metal level. The metallization process may be physical vapor deposition, for example.

These and other features of the present invention will be readily apparent to persons of ordinary skill in the art upon reading the entirety of this disclosure, which includes the accompanying drawings and claims.

#### DESCRIPTION OF THE DRAWINGS

10 FIG. 1 schematically illustrates the operation of an example physical vapor deposition process.

FIG. 2 schematically illustrates charge buildup on a gate of a logic module.

FIG. 3 shows a schematic diagram of a conventional circuit for protecting gates against charge buildup.

15 FIG. 4 shows a graph of the number of diodes as a function of a number of nets for an example device.

FIG. 5 schematically shows a layout of a conventional circuit for protecting gates against charge buildup.

FIG. 6 shows an equivalent schematic diagram for the diode cells in the layout of  
20 FIG. 5.

FIG. 7 shows a circuit for preventing charge buildup in accordance with an embodiment of the present invention.

FIG. 8 schematically illustrates a stacked via structure in accordance with an embodiment of the present invention.

FIG. 9 schematically shows a layout of a circuit for preventing charge buildup, in accordance with an embodiment of the present invention.

5        FIG. 10 shows a schematic diagram of an antenna diode for preventing charge buildup.

FIG. 11 shows a schematic diagram of a charge buildup protection transistor in accordance with an embodiment of the present invention.

10       FIG. 12 shows plots of the charge protection provided by the transistor of FIG. 11 compared to the antenna diode of FIG. 10.

FIG. 13 shows plots of current carrying capacities of a charge protection transistor and an antenna diode.

The use of the same reference label in different drawings indicates the same or like components. Drawings are not necessarily to scale unless otherwise noted.

15       DETAILED DESCRIPTION

In the present disclosure, numerous specific details are provided, such as examples of apparatus, components, and methods, to provide a thorough understanding of embodiments of the invention. Persons of ordinary skill in the art will recognize, however, that the invention can be practiced without one or more of the  
20       specific details. In other instances, well-known details are not shown or described to avoid obscuring aspects of the invention.

FIG. 7 shows a circuit 700 for preventing charge buildup on an interconnect line in accordance with an embodiment of the present invention. In the example of FIG. 7, circuit 700 protects the gate of a transistor 303, which may be a MOS transistor. Circuit 700 may include a transistor 703 and a capacitor 702. In one embodiment, transistor 5 703 comprises an N-type field effect transistor (nfet) with the source connected to ground and the drain connected to the metal wire that accumulates charge, which in this example is interconnect line 704. The gate of transistor 703 may be coupled to interconnect line 704 by way of capacitor 702. The gate of transistor 703 is otherwise left floating during the manufacture of the device including transistor 303. The gate of 10 transistor 703 may be subsequently connected to ground at a topmost metal level 706 of the device. That is, assuming interconnect line 704 is on M1 and the device has only three overlying metal levels M1, M2, and M3, the gate of transistor 703 may be left floating during the formation of M1, M2, and M3. The gate of transistor 703 may be later connected (see connection 705) to a quiet ground at M3 after M3 is formed. As 15 will be more apparent below, circuit 700 helps protect the gate of transistor 303 by preventing charge build-up on interconnect line 704 during formation of other metal wires, such as during the formation of M2 and M3 by a metallization process (e.g., physical vapor deposition). Grounding the gate of transistor 703 at the topmost metal level at a later processing step helps prevent transistor 703 from interfering with the 20 normal operation of transistor 303.

FIG. 8 schematically illustrates a stacked via structure in accordance with an embodiment of the present invention. In the example of FIG. 8, polysilicon 802 may comprise the gate of a charge buildup protection transistor, such as transistor 703.

Polysilicon 802 may be left floating during the formation of a first metal level 804 (i.e., an M1), a second metal level 806 (i.e., an M2), and other overlying metal levels. After the formation of the topmost metal level, polysilicon 802 may be coupled to ground at the topmost metal level by way of vias 803, 805, and other vias vertically stacked one on top of another between metal levels as shown in FIG. 8.

Referring back to FIG. 7, capacitor 702 may be a designed-in coupling or a parasitic capacitor. Capacitor 702 may be designed such that transistor 703 switches ON at about the threshold voltage (i.e.,  $V_T$ ) of transistor 703 to about the power supply voltage plus 20% (i.e.,  $V_T + 20\%$  of  $V_{CC}$ ). As charge accumulates on interconnect line 704, the gate of the transistor 703 starts to develop a voltage because of capacitor 702. This causes transistor 703 to start conducting current and discharge the accumulated charge on interconnect line 704, thereby protecting the gate of transistor 303. Note that the gate of transistor 703 is floating in the aforementioned circuit analysis. As mentioned, the gate of transistor 703 may remain floating until the topmost metal level is formed.

Circuit 700 may be implemented as a standard cell (for example, one per technology) that may be placed in lieu of antenna diode cells. FIG. 9 schematically shows such a layout in accordance with an embodiment of the present invention. In the example of FIG. 9, polysilicon 902 may be part of or connected to the gate of the charge buildup protection transistor (e.g. transistor 703). The gate of the charge buildup protection transistor may also comprise polysilicon. The charge buildup protection transistor may include a drain region 916, a source region 914, and a diffusion region 918. Drain region 916 is connected to interconnect line 904 by way of interconnect line

912. Only one charge buildup protection transistor is shown in FIG. 9 for clarity of illustration. In most applications, only one protection transistor may be needed.

Interconnect line 904 is connected to a node 906, which is connected to the net to be protected. A designed-in coupling or parasitic capacitor (e.g., capacitor 702) is

5 formed by interconnect line 904 over polysilicon 902. Interconnect line 904 may be on a first metal level, while polysilicon 902 may be directly under interconnect line 904 (e.g. see polysilicon 802 under first metal level 804 in FIG. 8). Interconnect line 904 and polysilicon 902 form parallel plates of the coupling capacitor. The characteristics of the coupling capacitor depends on a number of factors including the area of interconnect  
10 lines 904 and polysilicon 902, and the thickness of a dielectric layer between them.

Polysilicon 902 may be later coupled to a quiet ground on a topmost metal level by way of a via 920.

To minimize sub-threshold leakage, the length of the charge buildup protection transistor is preferably greater than the minimum allowable transistor length for the  
15 technology; for example, at least 2 times the minimum. As a particular example, if the minimum transistor length allowed is  $0.13\mu\text{m}$  (i.e.,  $0.13\mu\text{m}$  technology), then the length of the charge buildup protection transistor may be about  $0.26\mu\text{m}$  or higher. In an alternate embodiment, the designed-in coupling capacitor may be removed because the gate itself will accumulate charge. In an alternate embodiment, a high-threshold device  
20 may be used, such as a metal gate used in a diode configuration (source connected to gate), to prevent charge buildup on a metal wire. However, the threshold for such a device is so high that gate oxide breakdown may occur before the device turns on, rendering this embodiment less desirable than others. Sub-threshold leakage from a



minimum sized transistor may also be used to protect gates from charge buildup, but the resulting leakage may cause other problems.

FIG. 12 shows plots of the charge protection provided by a charge buildup protection transistor in accordance with an embodiment of the present invention compared to a conventional diode. In the example of FIG. 12, the horizontal axis represents time and the vertical axis represents voltage. Plot 1202 is for voltage readings at a node 1002 connected to a conventional diode 302 shown in FIG. 10. Plot 1206 is for voltage readings at a node 1102 of a charge buildup protection circuit shown in FIG. 11. The charge buildup protection circuit comprises a transistor 703 and a designed-in coupling capacitor 702 (see also FIG. 7). The gate of transistor 703 is connected to coupling capacitor 702, but is otherwise floating. Node 1102 is on interconnect line 704. In FIG. 12, plot 1204 is for voltage readings on node 701 between coupling capacitor 702 and the gate of transistor 703.

As shown in FIG. 12, coupling capacitor 702 may charge to about three volts before switching ON transistor 703. That corresponds to a peak voltage of about 8.5 volts on interconnect line 1102. In marked contrast, the conventional diode allows the voltage on node 1002 to reach over 14 volts and doesn't discharge as fast as the charge buildup protection transistor. Other advantages of the charge buildup protection transistor include reduced area, current leakage, and delay while providing more protection than conventional solutions. The transistor also provides an additional degree of freedom on the controllability of the voltage required to switch its floating gate ON.

A single small transistor can carry about 1000 times more current than a reverse biased diode (even after reverse diode breakdown). FIG. 13 shows plots of current carrying capacities over time. In FIG. 13, the horizontal axis represents time and the vertical axis represents current. Plot 1302 is for the current carrying capacity of a charge buildup protection transistor (e.g. transistor 703), while plot 1304 is for that of a conventional diode. As is evident in FIG. 13, the transistor has significantly more current carrying capacity than the diode.

While specific embodiments of the present invention have been provided, it is to be understood that these embodiments are for illustration purposes and not limiting.

Many additional embodiments will be apparent to persons of ordinary skill in the art reading this disclosure.